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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HARKNESS, CHARLES A	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/738,485	KORGER, PETER	
	Examiner	Art Unit	
	Charles A Harkness	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In view of Applicant's remarks respective to the title, the objection to the specification has been withdrawn.

Drawings

2. New corrected formal drawings in compliance with 37 CFR 1.121(d) are required in this application because the drawings in the application are informal drawings, and Applicant is required to provide the Office with formal drawings before the application can issue. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Vegesna et al, U.S. Patent Number 5,226,142 (herein referred to as Vegesna).

5. Referring to claims 1 and 15 Vegesna has taught a circuit comprising:

a register stack configured as (i) a plurality of segments addressable through a segment address signal and (ii) a plurality of registers within each of said plurality of segments, said

plurality of registers being addressable through a register address signal (Vegesna figure 6, figure 8; in figure 8, the register address signal is line are 90, while the segment address signal is made up of the signals coming from 106, 108, 110, and 112); and

a control circuit configured to (i) store a plurality of register states (Vegesna figures 6 and 8 column 2 lines 14-25; there are both global and local and shared registers present, therefore the system would have to be able to distinguish between the different states; column 10 lines 43-64; the result vector driver holds the different types of registers, or register states, and provides the incoming data to a certain register type based on the register address, the register states being global, shared, local), (ii) store a segment count signal (Vegesna column 3 lines 51-65; column 3 lines 32-36 – the CWP is the segment count; the pointer is incremented and decremented like a counter), and (iii) present said segment address signal responsive to said plurality of register states, said segment count signal, and said register address signal (Vegesna figure 8 numbers 90, 94, 98, 100, 68; the register address is fed in on line 90, the result vector driver 68 must keep track of which registers are in which states, so that it can determine which signals to operate and pass the data on, and the CWP, or window pointer then selects the 106 or 108 lines to turn on, in the case of a write to the registers).

6. Referring to claim 2 Vegesna has taught wherein at least one of said register states is fixed in a global state (Vegesna figure 6 and 8 column 2 lines 14-25).

7. Referring to claim 3 Vegesna has taught wherein at least one of said register states is fixed in a stackable state (Vegesna figure 6 and 8 column 2 lines 14-25).

8. Referring to claim 4 Vegesna has taught wherein said register stack further comprises:

a first portion disposed within a processor and configured as at least one segment of said plurality of segments; and

a second portion disposed external to said processor and configured as at least one segment of said plurality of segments (Vegesna figure 8; the local registers are a first portion of the segments, and the global registers are external to the local register segments).

9. Referring to claim 5 Vegesna has taught wherein said control circuit comprises:

a status circuit configured to present a gating signal responsive to said register address signal (Vegesna figure 8 number 76, the register address passes into the store register decode logic, which would be configured of logical gates, and the decode logic then presents a signal for register select, which would be from the logical gates, and thus would be a gating signal).

10. Referring to claim 6 Vegesna has taught wherein said status circuit comprises:

a comparator configured to present said gating signal responsive to said plurality of register states and said register address signal (Vegesna figure 8 column line 43-column 11 line 6; since the result vector driver 68 must decide which type of register lines to send the result through to the register file, based upon the register lines, the result vector driver must have a knowledge of which type, or state, a register is based upon its address, therefore the register state information must be stored in the result vector driver, and must be compared to the register address; the gating signal is then outputted as part of the segment address signal to the register file).

11. Referring to claim 7 Vegesna has taught wherein said status circuit comprises:

a memory device configured to store said plurality of register states and present said gating signal responsive to said plurality of register states and said register address signal

(Vegesna figure 8 column line 43-column 11 line 6; since the result vector driver 68 must decide which type of register lines to send the result through to the register file, based upon the register lines, the result vector driver must have a knowledge of which type, or state, a register is based upon its address, therefore the register state information must be stored in the result vector driver; the gating signal is then outputted as part of the segment address signal to the register file).

12. Referring to claim 8 Vegesna has taught wherein said plurality of logic gates are further configured to present said segment address signal as a predetermined address responsive to said gating signal having a global state (Vegesna figure 8 column line 43-column 11 line 6; since the result vector driver 68 must decide which type of register lines to send the result through to the register file, based upon the register lines, the result vector driver must have a knowledge of which type, or state, a register is based upon its address, therefore the register state information must be stored in the result vector driver; the gating signal is then outputted as part of the segment address signal to the register file based on the register state, or type being global, local, or shared).

13. Referring to claim 9 Vegesna has taught wherein said status circuit comprises:

a comparator configured to present said gating signal responsive to said plurality of register states and said register address signal (Vegesna figure 8 column line 43-column 11 line 6; since the result vector driver 68 must decide which type of register lines to send the result through to the register file, based upon the register lines, the result vector driver must have a knowledge of which type, or state, a register is based upon its address, therefore the register state information must be stored in the result vector driver, and must be compared to the register

address; the gating signal is then outputted as part of the segment address signal to the register file).

14. Referring to claim 10 Vegesna has taught a method of controlling a register stack comprising the steps of:

(A) comparing a register address with a plurality of register states to present a gating signal (Vegesna figure 8 column line 43-column 11 line 6; since the result vector driver 68 must decide which type of register lines to send the result through to the register file, based upon the register lines, the result vector driver must have a knowledge of which type, or state, a register is based upon its address, therefore the register state information must be stored in the result vector driver, and must be compared to the register address; the gating signal is then outputted as part of the segment address signal to the register file);

(B) gating a segment count with said gating signal to present a segment address (Vegesna column 3 lines 51-65; column 3 lines 32-36 – the CWP is the segment count; the pointer is incremented and decremented like a counter; figure 8 the lines making up the segment address signal 106 and 108 come from logic derived from the CWP, window pointer, and the gating signals from the result vector driver would be passed out on the lines of 91, 93, 95, and 97 as the other part of the segment address signal); and

(C) addressing said register stack with said register address and said segment address (Vegesna figure 8 numbers 90, 94, 98, 100, 68; the register address is fed in on line 90, which then drives the result vector driver 68 which sends out part of the segment address signal; and the CWP, or window pointer then selects the 106 or 108 lines to turn on, in the case of a write to the registers for the other part of the segment address signal).

15. Referring to claim 11 Vegesna has taught wherein step (A) further comprises the sub-steps of:

presenting a signal communicating said plurality of register states; and

selecting one of said plurality of register states as said gating signal based upon said register address (Vegesna figure 8 column line 43-column 11 line 6; since the result vector driver 68 must decide which type of register lines to send the result through to the register file, based upon the register lines, the result vector driver must have a knowledge of which type, or state, a register is based upon its address, therefore the register state information must be stored in the result vector driver; the gating signal is then outputted as part of the segment address signal to the register file based on the register state, or type being global, local, or shared).

16. Referring to claim 12 Vegesna has taught further comprising the step of:

setting said plurality of register states in response to a reset handler operation (Vegesna figure 8 column line 43-column 11 line 6; since the result vector driver 68 must decide which type of register lines to send the result through to the register file, knowing whether the type is global, local, or shared; in addition, when everything is cleared, the states of the registers would have to be set at some point, so the result vector driver knows which state each register is).

17. Referring to claim 13 Vegesna has taught further comprising the step of:

incrementing said segment address in response to a push instruction (Vegesna column 7 lines 5-15; the CWP operates as the window counter and is incremented and decremented based on calls and returns from subroutines).

18. Referring to claim 14 Vegesna has taught further comprising the step of: decrementing said segment address in response to a pop instruction (Vegesna column 7 lines 5-15; the CWP

operates as the window counter and is incremented and decremented based on calls and returns from subroutines).

19. Referring to claim 16 Vegesna has taught wherein said control circuit comprises:

A counter configured to present said segment count signal (Vegesna column 3 lines 51-65; the pointer is incremented and decremented like a counter; column 3 lines 32-36 – the CWP is the segment count).

20. Referring to claim 17 Vegesna has taught wherein said control circuit further comprises:

a plurality of logic gates configured to present said segment address signal responsive to said gating signal and said segment count signal (Vegesna figure 8 the lines making up the segment address signal 106 and 108 come from logic derived from the CWP, window pointer, and the gating signals from the result vector driver would be passed out on the lines of 91, 93, 95, and 97 as the other part of the segment address signal).

21. Referring to claim 18 Vegesna has taught the step of: presenting said segment address as a predetermined address responsive to said gating signal having a global state (Vegesna column 2 lines 15-25, figure 8 number 101; the segment count was already stored in the register as shown in column 3 lines 51-65; column 3 lines 32-36 – the CWP is the segment count; the pointer is incremented and decremented like a counter).

22. Referring to claim 19 Vegesna has taught wherein the step of: storing said register states prior to said comparing (Vegesna column 10 lines 43-64; the result vector driver holds the different types of registers, or register states, and provides the incoming data to a certain register type based on the register address, the register states being global, shared, local; since the result

vector driver is preloaded with the different types of registers, it would be stored prior to comparing).

23. Referring to claim 20 Vegesna has taught further comprising the step of: storing said segment count prior to said gating (Vegesna figure 8, column 12 line 37-column 13 line 9the segment address is "gated" through the "write decoded logic" and the "shared select logic" in figure 8 of Vegesna. Since the logic blocks are made up of logic gates, the segment count is gated through, with associated gating signals, the segment address is presented; the segment count was already stored in the register as shown in column 3 lines 51-65; column 3 lines 32-36 – the CWP is the segment count; the pointer is incremented and decremented like a counter).

Response to Arguments

24. Applicant's arguments filed 06/22/04 have been fully considered but they are not persuasive.

25. Applicant argue, in respect to the rejection of claims1 and 15:

> "...claim 1 provides (in part) a control circuit configured to store a plurality of register states. However, Vegesna appears to be silent regarding storing register states."

26. This is not persuasive. Looking to Vegesna column 10 lines 43-64; the result vector driver holds the different types of registers, or register states: global, shared, local, and provides the incoming data to the correct register and register state based on the register address.

27. Applicant argue, in respect to the rejection of claims 1 and 15:

> "Claim 1 further provides that the control circuit is configured to store a segment count signal. In contrast, Vegesna appears to be silent regarding storage of a signal similar to the claimed segment count signal."

28. This is not persuasive. Referring to Vegesna column 3 lines 32-36 and lines 51-65, the CWP is the segment counter, it is stored in a register and is incremented and decremented when the segments, or register windows, change. The register windows refer to the register "segments".

29. Applicant argue, in respect to the rejection of claims 1 and 15:

> "Vegesna states that the signals coming from the result vector driver 68 are data, not addresses."

30. The segment address signal is made up signals from 106, 108, 110, and 112 of figure 8, and they indicate which register segment, or register window is currently active.

31. Applicant argue, in respect to the rejection of claim 10:

> "Vegesna appears to be silent regarding register states."

32. This is not persuasive. Looking to Vegesna column 10 lines 43-64; the result vector driver holds the different types of registers, or register states: global, shared, local, and provides the incoming data to the correct register and register state based on the register address. The result vector driver's task is to provide the data to the correct register in the correct register state. Although Vegesna does not specifically call them register states, they are the functional equivalent, and only the naming is different.

33. Applicant argue, in respect to the rejection of claim 10:

> "Claim 10 further provides a step for gating a segment count with a gating count signal to present a segment address...the argument identifies sources of various signals, but never actually cites any evidence in Vegesna of a gating operation."

34. This is not persuasive. "Gating count signal" is not found anywhere in the claims, as described in Applicant's Remarks. In addition, the segment address is "gated" through the "write decoded logic" and the "shared select logic" in figure 8 of Vegesna. Since the logic blocks are made up of logic gates (column 12 line 37-column 13 line 9), the segment count is gated through, with associated gating signals, the segment address is presented.

35. Applicant argue, in respect to the rejection of claims:

"...Vegesna appears to be silent regarding any circuit presenting a gating signal."

36. This is not persuasive. Vegesna (figure 8 number 76) has taught that register address (ADDR R[5])passes into the store register decode logic, which would be configured of logical gates, and the decode logic then presents a signal for register select, which would be from the logical gates, and thus would be a gating signal.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579 and 571-272-4167 after 10/12/04. The examiner can normally be reached on 8Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Charles Allen Harkness

Examiner

Art Unit 2183

September 17, 2004